REMARKS

In the Official Action, the Examiner rejected claims 1-30. Claims 1, 4, 6, 9, 22 and 25 have been amended to set forth the recited subject matter more clearly. Applicant respectfully requests reconsideration of the application in view of the remarks set forth below. Applicant believes that all pending claims are in condition for allowance, as summarized below.

First, Applicant submits that the MacLaren reference does not anticipate any of the claims of the present application, because the MacLaren reference does not disclose each and every element recited in the present independent claims. *See infra.*, "Rejections Under 35 U.S.C. § 102." Second, Applicant submits that the MacLaren reference does not qualify as prior art against the present application under 35 U.S.C. §§ 102(e)/103, based on the common obligations of assignment of the present application and the MacLaren reference. *See infra.*, "Rejections Under 35 U.S.C. § 103."

Rejections Under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 1-15 and 22-30 under 35 U.S.C. § 102(e) as being anticipated by MacLaren (U.S. Patent No. 6,108,741). With specific regard to the independent claims, the Examiner stated:

> Regarding claims 1, 6, 9 and 12, discloses temporarily storing a plurality of transaction entries (e.g., col. 28, lines 34-37), selecting one of the plurality of temporarily stored transaction entries (e.g., col. 29, lines 64-66).
>
> Regarding claim 22, *MacLaren* discloses one processor and a memory device operatively coupled to the at least one processor (e.g., col. 5, lines 9-12); and a transaction order queue circuit configured to process transactions from the memory device, the transaction order queue circuit being adapted to encode a plurality of simultaneous transaction entries (e.g., col. 14, lines 22-23).

> Regarding claim 25, *MacLaren* discloses temporarily storing a plurality of simultaneous transaction entries (e.g., col. 14, lines 22-23); and delivering the plurality of transaction entries to a transaction order queue one at a time (e.g., col. 30, lines 30-37).
>
> Regarding claim 28, *MacLaren* discloses temporarily storing a plurality of simultaneous transaction entries (e.g., col. 14, lines 22-23); prioritizing each of the temporarily stored transaction entries; transmitting the stored transaction entries to the transaction order queue according to priority (e.g., col. 28, lines 34-44).

Applicant respectfully traverses these rejections. A *prima facie* case of anticipation under 35 U.S.C. § 102 requires a showing that each limitation of a claim is found in a single reference, practice or device. *In re Donohue*, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985). Anticipation under 35 U.S.C. § 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under 35 U.S.C. § 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

Independent claims 1, 6, 9 and 12 have been amended to set forth the recited subject matter more clearly. Generally, claims 1, 6 and 9 have been amended to clarify the intended scope by reciting aspects associated with prioritizing the transaction entries. Specifically, independent claim 1 recites "prioritizing each of the plurality of temporarily stored transaction

entries according to a bus standard," and "enqueuing...according to an associated priority." Independent claim 6 recites "providing logic to prioritize each of the plurality of transaction entries according to a bus standard," and "providing a transaction order queue...configured to receive the selected one of the plurality of temporarily stored transaction entries according to an associated priority determined by the prioritization logic." Independent claim 9 recites "means for prioritizing each of the plurality of temporarily stored transaction entries according to a bus standard," and "means for enqueuing...according to an associated priority determined by the prioritization means." Similarly, independent claim 12 recites "logic adapted for selecting and *ordering* the plurality of order transaction entries according to a bus standard." Independent claim 28 recites "temporarily storing a plurality of simultaneously received transaction entries" and "prioritizing each of the temporarily stored transaction entries."

Applicants respectfully submit that the MacLaren reference does not disclose prioritizing transaction entries according to a bus standard, such as PCI-X, or enqueuing according to the associated priority. The Examiner only cited col. 28, lines 34-37 and col. 29, lines 64-66 in support of the rejection under 35 U.S.C. §102. While it is unclear as to exactly which features of MacLaren the Examiner is associating with each of the presently recited elements, Applicants respectfully submit that the TRQ 2270 and TOQ 2272 discussed in the cited passages of MacLaren are not enqueued according to an associated priority. For instance, transactions in the TRQ 2270 are completed "in the order they were received." Col. 26, lines 63-65. Similarly, the TOQ 2272 is a first-in-first-out (FIFO) queue. Col. 28, lines 34-36. Even assuming that the TRQ and the TOQ disclosed in the MacLaren reference could be fairly correlated with the temporary storage element and/or the transaction order queue recited in the present claims, it is clear that the MacLaren reference does not disclose "prioritizing each of the plurality of temporarily stored transaction entries according to a bus standard" or

"enqueuing...according to an associated priority." Accordingly, the MacLaren reference does not disclose each and every element recited in independent claims 1, 6, and 9 or the subject matter of any claims dependent thereon. Further, the MacLaren reference does not disclose prioritizing a plurality of simultaneously received transaction entries, as recited in claim 28. Accordingly, the MacLaren reference does not disclose each and every element recited in independent claim 28 or the subject matter of any claims dependent theron.

Similarly, independent claim 12 recites "logic adapted for selecting and *ordering* the plurality of transaction entries." Emphasis added. In rejecting claim 12, the Examiner cited the same passages of the MacLaren reference, as discussed above with reference to claims 1, 6 and 9. As discussed above, Applicant respectfully submits that the MacLaren reference does not disclose prioritizing the temporarily stored transaction entries according to a bus standard in the context recited in the instant claims. Similarly, the MacLaren reference does not disclose logic adapted for ordering the plurality of transaction entries. There is no act of "ordering...according to a bus standard" in the TOQ or the TRQ. The TOQ and TRQ are simply enqueued as they are received. Accordingly, the MacLaren reference does not disclose each and every element recited in independent claim 12 or the subject matter of any claims dependent thereon.

Claims 22, 25 and 28 have been amended to more clearly set forth the novel feature of the present transaction order queue circuit and its ability to process simultaneously received transaction entries. Specifically, independent claim 22 recites a "transaction order queue circuit being adapted to encode a plurality of simultaneously received transaction entries." Claim 25 recites "temporarily storing a plurality of simultaneously received transaction entries." Claim 28 recites "temporarily storing a plurality of simultaneously received transaction entries." The Examiner cited col.14, lines 22 and 23 of MacLaren as disclosing this feature. The cited

passage of the MacLaren reference simply states that the tag memory 2036 "can handle up to four posted memory write transactions simultaneously." However, as stated in the MacLaren reference, "the tag memory 2036 is a circular FIFO device." Col.14, lines 21-22. Applicant respectfully submits that the statement regarding the tag memory's ability to "handle up to four posted memory write transactions simultaneously," simply means that the tag memory 2036 of the MacLaren reference can store up to four write transactions simultaneously. However, the tag memory 2036 is *not* configured to store or encode a plurality of *simultaneously received* transaction entries, as recited in claims 22, 25 and 28. Further, as discussed above, the MacLaren reference does not disclose prioritizing simultaneously received transaction entries, as further recited in claim 28. Accordingly, Applicant respectfully submits that the MacLaren reference does not disclose each of the elements recited in independent claims 22 and 25 or any of the claims dependent thereon.

Because the MacLaren does not disclose each of the elements recited in independent claims 1, 6, 9, 12, 22, 25 or 28, Applicant respectfully submits that these claims, as well as the claims dependent thereon, are not anticipated by the cited reference. Accordingly, Applicant respectfully requests withdraw of the Examiner's rejection and allowance of claims 1-15 and 22-30.

Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 16-21 under 35 U.S.C. § 103(a) as being unpatentable over MacLaren in view of Willenborg (U.S. Pat. No. 6,477,610). In view of the earlier date of invention of the subject matter disclosed and claimed in the present application, Applicant has chosen to remove the MacLaren reference pursuant to 37 C.F.R. § 1.131 and 35 U.S.C. §

103(c). Without the MacLaren reference, the Examiner's rejections under 35 U.S.C. § 103 cannot stand.

The MacLaren et al. reference (U.S. Pat. No. 6,108,741) was filed on June 5, 1996 and issued on August 22, 2000 ("the effective date"). Applicant submits that the presently recited subject matter was invented prior to the effective date of the MacLaren reference. Under 37 C.F.R. § 1.131, prior invention may be established in the United States, a NAFTA country, or a WTO member country by showing either (1) actual reduction to practice prior to the effective date of the MacLaren et al. patent, or (2) conception prior to the effective date of the MacLaren et al. patent coupled with diligence from prior to such date to a subsequent actual or constructive reduction to practice. Applicant has attached a declaration under 37 C.F.R. § 1.131 demonstrating that the present invention was conceived *before* the date of issue of the MacLaren reference and that applicant was diligent from before the effective date to filing the present application. To be clear, the Declaration is being submitted to establish that the claimed subject matter was invented prior to the *issue date* of the MacLaren reference. As such, the Declaration is sufficient to remove the MacLaren reference under 35 U.S.C. § 102(a), thus establishing that at best, the MacLaren reference is only available under 35 U.S.C. § 102(e).

As required by 37 C.F.R. § 1.131(b), the accompanying Declaration establishes a conception prior to the effective date of the MacLaren reference and due diligence from prior to the effective date of the MacLaren reference to the subsequent filing of the present application with the United States Patent and Trademark Office. In particular, the invention was conceived as early as February 4, 2000, as indicated on the invention disclosure (Declaration, para. 4 and Exhibit A). Due diligence is demonstrated by the following

documents; 1) a new file memo sent from Mike Fletcher acknowledging receipt of the invention disclosure and initiation of the preparation of the associated patent application transmitted to Compaq on August 16, 2000 (Declaration, para. 5 and Exhibit B); 2) billing record indicating numerous time entries corresponding to preparation of the application from August 31, 2000 to December 27, 2000 (Declaration, para. 6 and Exhibit C); 3) a letter transmitting the first draft of the application to the inventor on December 28, 2000 (Declaration, para. 7 and Exhibit D). The constructive reduction to practice is demonstrated by the filing of the final draft of the patent application on February 8, 2001, as evidenced by the attached filing receipt (Declaration, para. 8 and Exhibit E).

In view of these facts, it is clear that the invention was conceived at least as early as February 4, 2000 and due diligence was exercised from at least August 16, 2000, which is a week prior to the effective date of August 22, 2000, through the constructive reduction to practice of the invention on February 8, 2001.

As a result of the prior invention date, the MacLaren reference is only available as prior art under 35 U.S.C. § 102(e)/103(a). However, Applicant submits that the MacLaren reference is unavailable as prior art under 35 U.S.C.§103(c). Applicant respectfully refers the Examiner to 35 U.S.C. § 103(c) which states:

> Subject matter developed by another person, which qualifies as prior art under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

In accordance with 35 U.S.C. § 103(c) and Pub. L. 106-113, § 4807, enacted November 29, 1999, subject matter developed by another person which qualifies as prior art

only under subsection (e) of 35 U.S.C. § 102, shall not preclude patentability where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Here, the MacLaren reference and the claimed invention were, at the time the invention was made, owned or subject to an obligation of assignment to Compaq Information Technologies Group, L.P. The present assignee is Hewlett-Pakard Development Company, L.P., a wholly owned affiliate of Hewlett-Packard Company. Since the present application was filed after November 29, 1999 and based on the forgoing discussion, it is clear that the MacLaren reference does not qualify as prior art under 35 U.S.C. § 102(e)/103(c).

Without the MacLaren reference, the Examiner's rejection under 35 U.S.C. § 103 is moot, since it is clear that none of the art of record that is available as prior art, either alone or in combination, discloses or suggests all of the elements recited in the present claims. Accordingly, Applicant respectfully requests withdrawal of the Examiner's rejection and allowance of claims 16-21. Further, based on the discussion above with respect to the rejections under 35 U.S.C. § 102, Applicant respectfully submits that claims 1-15 and 22-30 are not anticipated by the MacLaren reference, and further submit that any future rejections of claims 1-15 and 22-30 under 35 U.S.C. § 103 based on the MacLaren reference would be improper since the MacLaren reference is not available as prior art under 35 U.S.C. § 102(e)/103(c).

Conclusion

In view of the remarks and amendments set forth above, Applicant respectfully requests allowance of the pending claims 1-30. If the Examiner believes that a telephonic

interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: January 18, 2005

Robert A. Manware
Reg. No. 48,758
(281) 970-4545

Correspondence Address:
Hewlett-Packard Company
IP Administration
Legal Department, M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400

EXHIBIT "A"

CONFIDENTIAL – NEED TO KNOW REQUIRED

COMPAQ®

Comp: 0187

(for Legal Dept. use only)
ID No: P00-3008
Date Received: 4 FEB 2000

INVENTION DISCLOSURE FORM

PREPARED AND SUBMITTED AT THE REQUEST AND DIRECTION OF AN ATTORNEY
RETURN COMPLETED FORM TO DIANE STRONG

1. DESCRIPTIVE TITLE OF INVENTION: Enhancement to Transaction Order Queue

2. INVENTOR (S): More than two? ☐ Yes ☒ No. (If more than two, use last page.)

A.

Last Name	Given First Name	Nickname (if any)	Middle Initial/Name
Shah	Paras		A
Home Street Address		Home Phone	Pager Number
10738 North Belmont Court		281-955-8224	
City	State	Zip	Citizenship
Houston	TX	77065	USA
Work Phone	Work Fax	Mail Code	Employee #
281-514-2432	281-518-1134	090610	20609
Name of Supervisor		Name of Employer (if NOT an employee of Compaq)	
John MacLaren			

GROUP	DIVISION
☐ CON	☐ Presario Mobile; ☐ Peripherals; ☐ Desktop; ☐ Internet Services; ☐ Con. Adv. Tech.
☒ ESSG	☒ Industry Standard Servers; ☐ Storage Products; ☐ Telecommunications; ☐ High Perf. Server Bus. Unit; ☐ Unix Bus. Unit; ☐ NonStop e-business; ☐ Compaq Services; ☐ Professional Services; ☐ Alpha; ☐ Tandem Bus. Unit
☐ CPCG	☐ Workstations; ☐ Desktop; ☐ Displays & Peripherals; ☐ Portables; ☐ Small & Medium Business
☐ MFG	
☐ TCD	☐ Research & Development

B.

Last Name	Given First Name	Nickname (if any)	Middle Initial/Name
Home Street Address		Home Phone	Pager Number
City	State	Zip	Citizenship
Work Phone	Work Fax	Mail Code	Employee #
Name of Supervisor		Name of Employer (if NOT an employee of Compaq)	

GROUP	DIVISION
☐ CON	☐ Presario Mobile; ☐ Peripherals; ☐ Desktop; ☐ Internet Services; ☐ Con. Adv. Tech.
☐ ESSG	☐ Industry Standard Servers; ☐ Storage Products; ☐ Telecommunications; ☐ High Perf. Server Bus. Unit; ☐ Unix Bus. Unit; ☐ NonStop e-business; ☐ Compaq Services; ☐ Professional Services; ☐ Alpha; ☐ Tandem Bus. Unit
☐ CPCG	☐ Workstations; ☐ Desktop; ☐ Displays & Peripherals; ☐ Portables; ☐ Small & Medium Business
☐ MFG	
☐ TCD	☐ Research & Development

3. **CONCEPTION OF INVENTION:**

A. When did you first think of this invention? _____

B. Date of first written description? _____

C. Please attach the first written description. (If submitting in electronic format, please scan all attachments and send).

D. If you can not send the first written description, please explain why and state where it can be found. _____

E. Please list the name of others in Compaq to whom you've described the invention:

_____

4. **IMPLEMENTING THE INVENTION**

A. Has the invention been implemented? ☒ Yes ☐ No ☐ Don't know
(Implementations can include physical prototypes, software, models, and simulations)

B. If implemented, please do not destroy, alter, or modify the implementation(s) without the authorization of the Compaq Legal Department, and answer the following questions for each implementation.

i. When was it implemented? _____
ii. Where is the implementation now? (Attach or scan and send photograph, if possible)
iii. Has the implementation been tested? Yes
iv. If so, was the test successful? Yes

5. **USE OR SALE OF INVENTION:**

A. Has this been or will this be incorporated into a Compaq product? ☒ Yes ☐ No
If so, for each such product identify:

i. When was it or will it be incorporated into the product? _____
ii. Code name: _____

B. Has the invention been offered for sale or sold to anyone (e.g. an end user, vendor, reseller, partner, etc.)
☐ Yes ☐ No ☒ Don't know

i. If so, when: _____
ii. If so, to whom (name of company or individual): _____

C. If you don't know whether the invention has been offered for sale, or sold please state who is the best person to contact to determine when the invention has been or will be offered for sale or sold: _____

NOTE: Please inform Compaq Legal immediately if, in the future, any of your answers under this Section 5 change so that we have ample opportunity to protect the invention within the time limits set out by law.

6. **DISCLOSURE OF INVENTION TO OTHERS:**

A. Has a disclosure of the invention been made to any person(s) who is **NOT** a Compaq employee (including contractor, temporary, vendor, reseller, or partner and including conference presentations or journal articles)?
☐ Yes ☒ No ☐ Don't know

B. If a disclosure was made, when was it made? _____

C. To whom was the disclosure made? _____

D. Was the disclosure made under an obligation of confidence? (e.g. Nondisclosure Agreement)
☐ Yes ☐ No ☐ Don't know

7. **DESCRIPTION OF THE INVENTION** (continue on extra sheets, as necessary)

A. What type of technology does your invention relate to? (Check all that apply)

CPU Technologies
- ☐ Keyboard/Mouse/other input device
- ☐ Graphics
- ☒ Architecture
- ☐ Audio
- ☐ Memory
- ☒ Buses (ISA, EISA, PCI, AGP, other)
- ☐ Power Supplies/Batteries
- ☐ Other: _____

Communications Technologies
- ☐ Network Interface Card
- ☐ Hubs/Concentrators
- ☐ Routers
- ☐ Switches
- ☐ Modems
- ☐ Remote Access
- ☐ Other: _____

Peripherals Technologies
- ☐ Monitors/Screens
- ☐ CD-ROM
- ☐ DVD
- ☐ Tape Drives
- ☐ Disk Storage Systems
- ☐ Disk Controllers
- ☐ Printers
- ☐ Storage
- ☐ Other: _____

Feature/Software Technologies
- ☐ Mulitprocessor
- ☐ Fault Tolerance
- ☐ Remote Control
- ☐ Power Management
- ☐ Security
- ☐ Intelligent Manageability
- ☐ Smartstart
- ☐ Insight Manager
- ☐ Other _____

Other
- ☐ Manufacturing Processes
- ☐ Mechanical (functional)
- ☐ Mechanical (ornamental)
- ☐ PC/TV
- ☐ Racks
- ☐ Other: _____

B. Describe the general subject matter of the invention: The invention deals with an enhancement to a transaction order queue. A transaction order queue (TOQ) is used to store the relative order of transactions flowing through a bridge ASIC. A TOQ is required for ASICs that have multiple transactions outstanding and can schedule between them. The TOQ allows the queuing of many transactions within a single device, and ensures PCI/PCI-X ordering rules are not violated.

C. Describe the particular problem faced by those working in the subject matter area: For today's complicated server ASICs, the depth of the TOQ can be large (>20 entries). Due to the depth of the queue, typically only one entry can be enqueued in a particular clock cycle. Modifying the TOQ to enqueue multiple events per cycle significantly increases complexity, and may not be possible with the high clock speed requirements of current chips.

This limitation is problematic in applications where multiple events may be received in a single clock cycle. These situations frequently occur in application. For example, if one side of the device is operating at a higher frequency, then it may send multiple events across in a single clock period of the slower side of the device. Also, there are applications where the sender may actually want to send multiple unrelated events in a single clock cycle. In these situations, the enhancement described below maintains transaction ordering while allowing multiple events to be stored.

D. Describe the old method(s) of performing the functions of the invention: Previously, ad hoc approaches were used to "patch" the problem. These solutions were designed to work for particular cases the target device would be exposed to. As new bus types (ex. PCI-X) and bus frequencies increase, these solutions no longer function properly.

E. Why is the invention better than these old approaches? This invention is a general purpose block that can be added to the front of the TOQ. It can handle many more combinations of events than the previous solutions, allowing it to be used in applications such as PCI-X. The invention is localized to the TOQ itself, so other logic blocks can enqueue events as they happen without any special modification.

F. Attach at least one drawing or sketch of the invention if available. (Attach or scan and send drawing or sketch)

G. Describe the invention, how it is used, and how it operates: For each new event that occurs, store the event in a small bank of registers. These registers do not maintain ordering information, but do store the type of cycle (read request, write request, or read completion). For read completions, additional bits store which cacheline the completion references. Dequeue one entry per clock cycle into the transaction order queue, with the restriction that write requests, if present, must always be dequeued first. This dequeue order guarantees that PCI ordering rules will not be violated, and ensures that only one entry will be enqueued into the transaction order queue within a single clock cycle.

Since a single buffer only enqueues at most one event per cacheline (or one event total for write requests and read requests), there is no possibility of the register bank overflowing.

Under normal circumstances, no additional latency is experienced by using the enhancement. Only under infrequent cases such as a transaction being enqueued

coincident with the transaction order queue dequeueing its last entry will there be additional latency. Even in this rare case, the additional latency is only one clock cycle.

H. Describe the construction and structure of the preferred implementation of the invention: The invention consists of a bank of registers and associated combinatorial logic that sit in front of the main TOQ. These registers can enqueue mutilple events per clock but dequeue only one entry into the TOQ per clock. All logic that composes the invention can be placed into the module containing the TOQ. This localizes the block and allows the other modules to function without modification. The logic would be fabricated as part of the ASIC in functions in.

I. Is the invention designed to conform or enhance any industry standard?
☒ Yes ☐ No ☐ Don't Know
If so, what industry standard? PCI, PCI-X Specification

INVENTOR(S) SIGNATURE(S):

Pavan Shah
INVENTOR
Date: 2/1/2000

INVENTOR
Date:

INVENTOR
Date:

INVENTOR
Date:

ADDITIONAL INVENTORS:

C.

Last Name	Given First Name	Nickname (if any)	Middle Initial/Name
Home Street Address		Home Phone	Pager Number
City	State	Zip	Citizenship
Work Phone	Work Fax	Mail Code	Employee #
Name of Supervisor		Name of Employer (if NOT an employee of Compaq)	

GROUP	DIVISION
☐ CON	☐ Presario Mobile; ☐ Peripherals; ☐ Desktop; ☐ Internet Services; ☐ Con. Adv. Tech.
☐ ESSG	☐ Industry Standard Servers; ☐ Storage Products; ☐ Telecommunications; ☐ High Perf. Server Bus. Unit; ☐ Unix Bus. Unit; ☐ NonStop e-business; ☐ Compaq Services; ☐ Professional Services; ☐ Alpha; ☐ Tandem Bus. Unit
☐ CPCG	☐ Workstations; ☐ Desktop; ☐ Displays & Peripherals; ☐ Portables; ☐ Small & Medium Business
☐ MFG	
☐ TCD	☐ Research & Development

D.

Last Name	Given First Name	Nickname (if any)	Middle Initial/Name
Home Street Address		Home Phone	Pager Number
City	State	Zip	Citizenship
Work Phone	Work Fax	Mail Code	Employee #
Name of Supervisor		Name of Employer (if NOT an employee of Compaq)	

GROUP	DIVISION
☐ CON	☐ Presario Mobile; ☐ Peripherals; ☐ Desktop; ☐ Internet Services; ☐ Con. Adv. Tech.
☐ ESSG	☐ Industry Standard Servers; ☐ Storage Products; ☐ Telecommunications; ☐ High Perf. Server Bus. Unit; ☐ Unix Bus. Unit; ☐ NonStop e-business; ☐ Compaq Services; ☐ Professional Services; ☐ Alpha; ☐ Tandem Bus. Unit
☐ CPCG	☐ Workstations; ☐ Desktop; ☐ Displays & Peripherals; ☐ Portables; ☐ Small & Medium Business
☐ MFG	
☐ TCD	☐ Research & Development

E.

Last Name	Given First Name	Nickname (if any)	Middle Initial/Name
Home Street Address		Home Phone	Pager Number
City	State	Zip	Citizenship
Work Phone	Work Fax	Mail Code	Employee #
Name of Supervisor		Name of Employer (if NOT an employee of Compaq)	

GROUP	DIVISION
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☐ ESSG	☐ Industry Standard Servers; ☐ Storage Products; ☐ Telecommunications; ☐ High Perf. Server Bus. Unit; ☐ Unix Bus. Unit; ☐ NonStop e-business; ☐ Compaq Services; ☐ Professional Services; ☐ Alpha; ☐ Tandem Bus. Unit
☐ CPCG	☐ Workstations; ☐ Desktop; ☐ Displays & Peripherals; ☐ Portables; ☐ Small & Medium Business
☐ MFG	
☐ TCD	☐ Research & Development

EXHIBIT “B”

DATE: AUGUST 16, 2000

VIA E-MAIL

To: Diane H. Strong

From: Michael G. Fletcher

Re: **NEW FILE MEMO**

Preliminary Title: Enhancement to Transaction Order Queue

Preliminary Inventor(s): Paras A. Shah

Group/Division: ESSG/ISS
Compaq Houston

Invention Disclosure No:
(if applicable)

Compaq Docket No: P00-3008

Type of Application: _X_ Regular ____ Continuation ____ CIP ____ Divisional

Firm Matter No.: COMP:0187

Working Attorney: Mike Fletcher

Estimated Hourly Billing:

EXHIBIT “C”

Client	Trans Date	Tmkr	H P	Tcode/ Task Code	Stmt # Rate	Hours to Bill	Amount		Ref #
Client ID COMP.0187 Hewlett-Packard Company									
COMP.0187	08/31/2000	2	A	1		1.20		conference with inventor re disclosure.	ARCH
COMP.0187	08/31/2000	19	A	1		0.40		Review disclosure.	ARCH
COMP.0187	08/31/2000	19	A	1		1.20		Meeting with Paras Shea and review additional disclosure.	ARCH
COMP.0187	09/01/2000	19	A	1		0.75		Begin patent application. Organize background and diagrams. Reviewed subject matter.	ARCH
COMP.0187	09/05/2000	19	A	1		1.50		Review technology and begin preparing application background.	ARCH
COMP.0187	09/06/2000	19	A	1		2.30		Telephone conference with Paras Shah. Prepare background material.	ARCH
COMP.0187	09/11/2000	19	A	1		2.00		Draft claims.	ARCH
COMP.0187	09/12/2000	2	A	1		1.50		attorney conference re claim preparation.	ARCH
COMP.0187	09/12/2000	19	A	1		1.50		Review application and technology with attorney.	ARCH
COMP.0187	09/13/2000	2	A	1		0.80		attorney conference re preparation of background, specification, and drawings.	ARCH
COMP.0187	09/13/2000	19	A	1		2.50		Organize figures for application and draft claims.	ARCH
COMP.0187	09/15/2000	2	A	1		0.50		Review preparation of application.	ARCH
COMP.0187	09/26/2000	19	A	1		3.50		Draft claims for patent application.	ARCH
COMP.0187	09/27/2000	19	A	1		0.75		Draft claims for patent application.	ARCH
COMP.0187	09/29/2000	19	A	1		1.75		Review and draft background and specification.	ARCH
COMP.0187	10/02/2000	19	A	1		0.50		Discussed background and specification with Paras. Review and broadening of claims according to Paras suggestions.	ARCH
COMP.0187	10/06/2000	19	A	1		2.40		Draft background and revise application.	ARCH
COMP.0187	10/09/2000	19	A	1		2.00		Prepare background and specification.	ARCH
COMP.0187	10/10/2000	19	A	1		0.70		Draft specification and prepare drawings.	ARCH
COMP.0187	10/11/2000	19	A	1		1.00		Draft patent application and prepare drawings.	ARCH
COMP.0187	10/12/2000	19	A	1		0.40		Draft patent application claims.	ARCH
COMP.0187	10/28/2000		A	91				Regular Payment	ARCH
COMP.0187	11/14/2000	19	A	1		6.00		Draft claims and patent application.	ARCH
COMP.0187	11/15/2000	19	A	1		4.50		Revise application and add claims.	ARCH
COMP.0187	11/16/2000	19	A	1		2.30		Revise claims and application.	ARCH
COMP.0187	11/20/2000		A	91				Regular Payment	ARCH
COMP.0187	11/21/2000	2	A	1		3.30		review and revise draft application.	ARCH
COMP.0187	11/22/2000	19	A	1		1.50		Revise patent application.	ARCH
COMP.0187	11/27/2000	19	A	1		1.60		Revise patent application and amend claims.	ARCH
COMP.0187	11/28/2000	19	A	1		1.10		Revise application and claims.	ARCH
COMP.0187	11/29/2000	19	A	1		2.80		Revise claims and prepare for review by inventor.	ARCH
COMP.0187	11/30/2000	2	A	1		1.70		review and revise draft application.	ARCH
COMP.0187	12/04/2000	19	A	1		0.70		Revise claims of application.	ARCH
COMP.0187	12/05/2000	19	A	1		0.60		Revise draft application. Draft detailed description on Fig. 3.	ARCH
COMP.0187	12/08/2000	19	A	1		2.10		Revise Figure and draft detailed description with new figure from inventor and revise claims.	ARCH
COMP.0187	12/21/2000	2	A	1		1.00		review and revise draft application.	ARCH
COMP.0187	12/22/2000		A	91				Regular Payment	ARCH
COMP.0187	12/26/2000	19	A	1		1.00		Revise draft application.	ARCH
COMP.0187	12/27/2000	19	A	1		2.50		Revise draft application and re-draft figures. Telephone conference with inventor regarding figures.	ARCH
COMP.0187	12/28/2000	2	A	48				Federal Express.	ARCH
COMP.0187	01/27/2001		A	91				Regular Payment	ARCH
COMP.0187	01/31/2001	2	A	48				Federal Express.	ARCH
COMP.0187	01/31/2001	2	A	52				Federal Express.	ARCH
COMP.0187	02/08/2001	2	A	56				Express Mail.	ARCH
COMP.0187	02/08/2001	2	A	74				Patent Application Filing Fee and Assignment Recording Fee	ARCH
COMP.0187	02/24/2001		A	91				Regular Payment	ARCH
Total for Client ID COMP.0187					Billable Payments	61.85			
								Hewlett-Packard Company Enhancement to Transaction Order Queue	
						GRAND TOTALS			
					Billable Payments	61.85			

EXHIBIT "D"

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December 28, 2000

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P.O. Box 692000
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P00-3008 – 1st Draft of Application

U.S. Patent Application Serial No.: Not Assigned
Formal Title: Enhancement to Transaction Order Queue
Inventor(s): Paras Shah
Group: ESSG Division: ISS Compaq: Houston
CPQ Ref. No.: P00-3008 Firm Ref. No.: COMP:0187
Patent Engineer:

Dear Diane:

Attached is the first Draft patent application and drawings which was sent to Paras Shah for review.

If you have any questions or comments, please do not hesitate to contact me.

Sincerely yours,

Michael G. Fletcher

MGF:lh
Attachment

EXHIBIT "E"

UNITED STATES PATENT AND TRADEMARK OFFICE

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COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/779,424	02/08/2001	2171	1290	COMP:0187	4	30	8

CONFIRMATION NO. 5601

FILING RECEIPT

OC000000005849635

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Date Mailed: 03/12/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the PTO processes the reply to the Notice, the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Paras A. Shah, Houston, TX;

Continuing Data as Claimed by Applicant

Foreign Applications

If Required, Foreign Filing License Granted 03/10/2001

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No

Title

Enhancement of transaction order queue

Preliminary Class

707

Data entry by : MOHAMED, RIZAHA Team : OIPE Date: 03/12/2001

[redacted]